What is Claimed is:

1. A method of accessing a memory core more than once in a single clock cycle.

2. The method of Claim 1, wherein said more than once is twice.

3. The method of Claim 1, wherein said more than once is at least three times.

4. The method of Claim 2, wherein said memory core is incorporated into a dual-access RAM.

5. The method of Claim 1, wherein self-timing logic is used to facilitate accessing a memory core more than once in a single clock cycle.

6. The method of Claim 5, wherein said self-timing logic is implemented in a memory wrapper coupled to said memory core.

7. The method of Claim 6, wherein said memory wrapper couples said memory core to a memory interface unit.

8. The method of Claim 1, wherein said memory core is part of a processing engine.

9. The method of Claim 1, wherein said memory core is a single access memory core.

10. The method of Claim 1, wherein said memory core is part of the processor core.

11. An electronic device, comprising:

a memory core; and

circuitry coupled to said memory core for accessing said memory core more than once in a single clock cycle.

12. The device of Claim 11, wherein said memory core is part of a dual-access RAM.

13. The device of Claim 11, wherein said memory core and said circuitry combine to form a multiple access memory core.

14. The device of Claim 11 wherein said circuitry is embodied in an electronic device coupling a memory interface unit to said memory core.

15. The device of Claim 11, wherein said memory interface unit couples a central processing unit to said electronic device which couples said memory interface unit to said memory core

16. The device of Claim 11, wherein said electronic device is a digital signal processor.

17. The device of Claim 11, wherein said memory core is part of the processor core.

18. An electronic system, comprising:

at least one input/output device; and

an integrated circuit, coupled to the at least one input/output device, and comprising:

functional circuitry, for executing logical operations upon digital data signals in a synchronous fashion according to an internal clock signal;

power distribution circuitry, coupled to a battery, for distributing power to the functional circuitry; and

circuitry coupled to a memory core in said integrated circuit for accessing said memory core more than once in a single clock cycle.